

REMARKS

Claims 1-3 are pending. Claims 4-18 have been previously cancelled. Claims 1 and 2 have been amended. No new matter has been introduced. Reexamination and reconsideration of the application are respectfully requested.

In the October 19, 2004 Office Action, the Examiner rejected claims 1 and 3 under 35 U.S.C. §103(a) as being obvious over Makino, U.S. Patent No. 6,635,935 (hereinafter the Makino reference), in view of Kinoshita, U.S. Patent No. 5,869,852 (hereinafter the Kinoshita reference). This rejection is respectfully traversed.

The Examiner objected to claim 2 as being dependent upon a rejected base claim, but indicated that such claim would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. By this amendment, Applicant has rewritten claim 2 in independent form in accordance with the Examiner's remarks. Applicant believes that rewritten independent claim 2 is in condition for allowance.

Independent claim 1, as amended, recites:

A semiconductor integrated circuit device comprising:

a semiconductor substrate defining a plurality of rows, each row including areas for a sequence of cells;

a plurality of active regions disposed in each of said rows constituting semiconductor elements of associated cells;

at least one wiring region of a stripe shape elongated along a direction of a row, defined on said semiconductor substrate outside of said active regions in each row, and including wirings belonging to the associated cells, each wiring region having height, so

that the wiring region in a same row has a varying height from a first location position to a second location position in a direction crossing the row direction, the at least one wiring region having a locally varying height.

The Examiner rejected claims 1 and 3 under 35 U.S.C. §103(a) as being obvious over the Makino reference, in view of the Kinoshita reference. In so doing, the Examiner stated "Makino fails to disclose the required wiring/interconnected region varying width configuration. However, Kinoshita discloses a semiconductor integrated circuit and semiconductor integrated circuit layout designed by cell base system where in Columns 6 and 7, the required varying wiring/interconnect region configuration is disclosed."

The reference and the Kinoshita reference do not disclose, teach, or suggest the semiconductor integrated circuit specified in independent claim 1, as amended. Unlike the semiconductor integrated circuit specified in independent claim 1, as amended, the Makino reference and the Kinoshita reference do not show that **"the wiring region in a same row has a varying height from a first location position to a second location position in a direction crossing the row direction, the at least one wiring region having a locally varying height"**.

The Kinoshita reference states "the wiring channel 17 is a wiring region between the adjacent cell rows 11 having a height that varies depending on the crowdedness of the wiring pattern in the wiring channel 17, which is different from that in a gate array system. That is, if the degree of crowdedness is high, **the height of the wiring channel 17 is expanded and, by contrast, when the degree of crowdedness is low, the height of the wiring channel 17 is shrunk.**" (Col. 6, lines 60-67.)

The Kinoshita reference does not disclose, teach, or suggest the semiconductor integrated circuit specified in independent claim 1, as amended. The Kinoshita reference does not show that “the wiring region in a same row **has a varying height from a first location position to a second location position** in a direction crossing the row direction, the at least one wiring region having **a locally varying height**”.

Accordingly, the Applicant respectfully submits that independent claim 1, as amended, distinguishes over the above-cited references. Claim 3 depends directly from independent claim 1, as amended. Therefore, Applicant respectfully submits that claim 3 distinguishes over the above-cited references for the same reasons as set forth above with respect to independent claim 1, as amended.

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Applicant believes that the foregoing amendment and remarks place the application in condition for allowance, and a favorable action is respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the examiner believe that such a telephone conference would advance prosecution of the application.

Respectfully submitted,

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